74th Electronic Components and Technology Conference/ECTC

IEEE EPS Seminar, Challenges of Chiplets on Large Substrates

Advanced Substrate Materials for Large Substrate

RESONAC

May 28th 2024

Resonac Corporation

Today's Contents

- *Introduction*
- *Update*
  - *-Motivation and Challenges in Semiconductor*
  - *-Material Development Direction*
  - *-Latest Status of Material Development*
- *Needs of Organic Core for Large Substrate*

January 2023: Resonac was born

RESONAC

Showa Denko

Showa Denko Materials
(Former Hitachi Chemical)

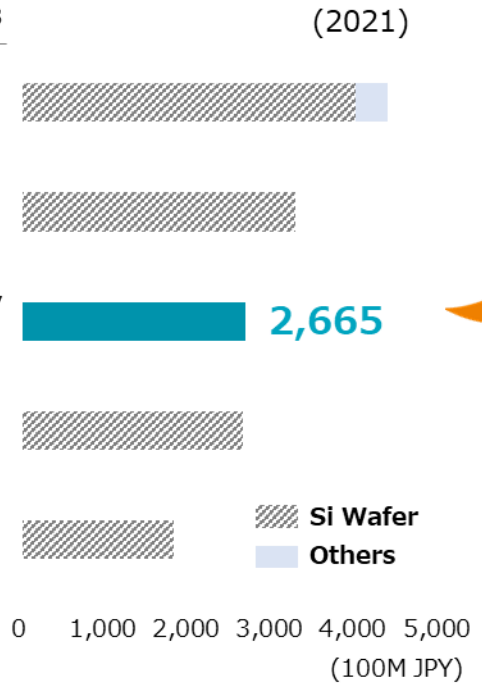
RESONAC

Chemistry for Change

Top Company in Semiconductor Related Materials

Global Players and Sales in Semiconductor Related Materials

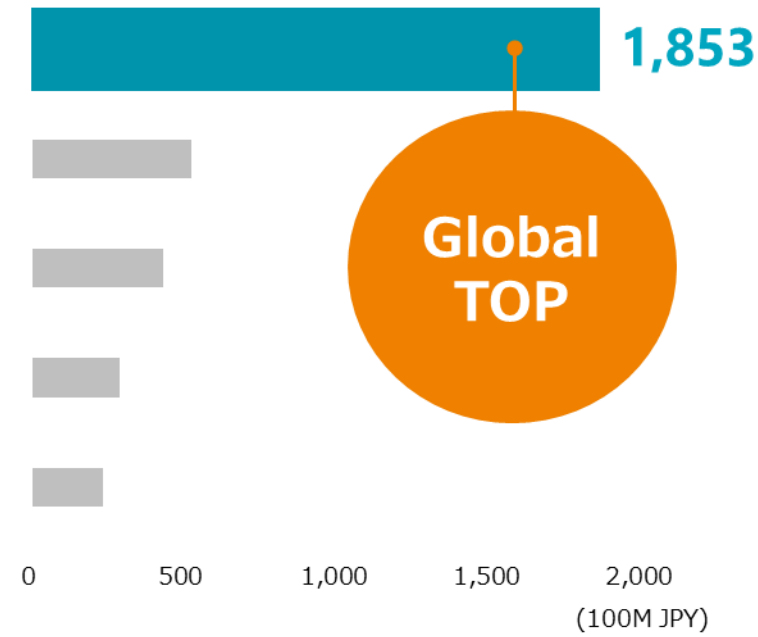
Company	Main Products
A	Si Wafer
B	Si Wafer
RESONAC	High-purity gas, CMP, Back-End Materials
C	Si Wafer
D	Si Wafer



Source : Showa Denko's original survey (except for SiC business)

Materials for Back-end Process (Semiconductor Packaging Process)

Company	Main Products
RESONAC	CCL (No.1) DAF (No.1) DFR (No.1) EMC (No.2)
E	CCL for PKG
F	CCL, EMC, DAF, Photosensitive Materials
G	CCL for PKG
H	CCL for PKG EMC



Resonac Materials Lineup for Semiconductor

RESONAC

Front-end Process

Wafer

Depo-sition | Photoli-thography | Etching | CMP | Buffer coat RDL

- High-purity Solvent
- High-purity Gas — Global 1st 43% for Etching
- CMP Ceria Slurry — Global 1st 50%
- PID — Global 1st 32% *HDM

Substrate manufacturing

Core Patterning | Drill TH Plating | Build-up | Solder mask | Solder/Cu Bumping

- Core material CCL — Global 1st 88% for PKG
- Dry film resist — Global 1st 52%
- Solder resist — Global 1st 85% for FC-BGA

Back-end Process

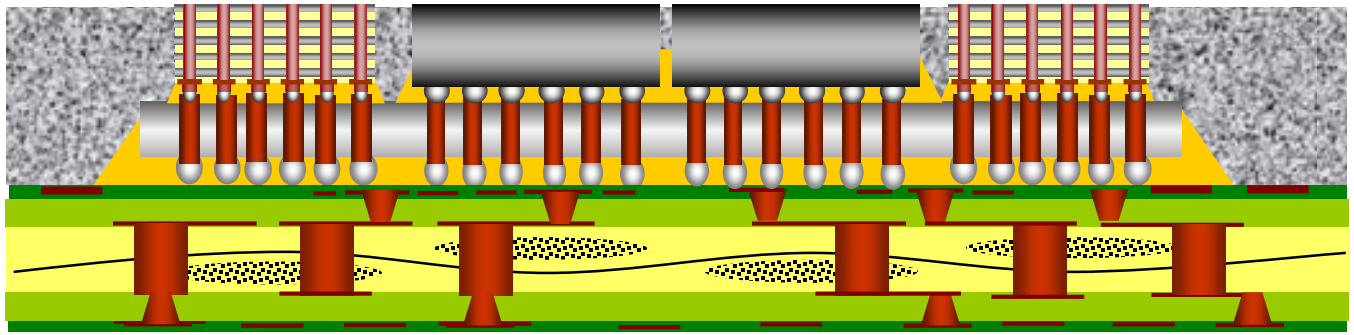
Package

Dicing | Si–Interposer | HBM Mounting | Bonding Underfill | Molding Dicing | Bonding Substrate | Heat-sink attach

- Die bonding film NCF — Global 1st 47%
- CUF MUF — Global 2nd 19%
- EMC — Global 2nd 19%
- TIM — Sheet type 100%

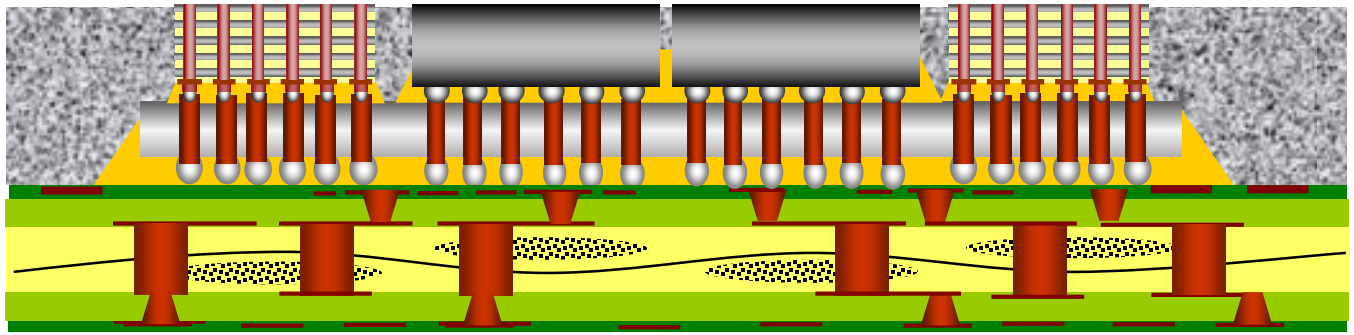
*1 Global market shares are based on data gathered by RESONAC
*2 HDM: HD Microsystems

Motivation and Challenges in Semiconductors



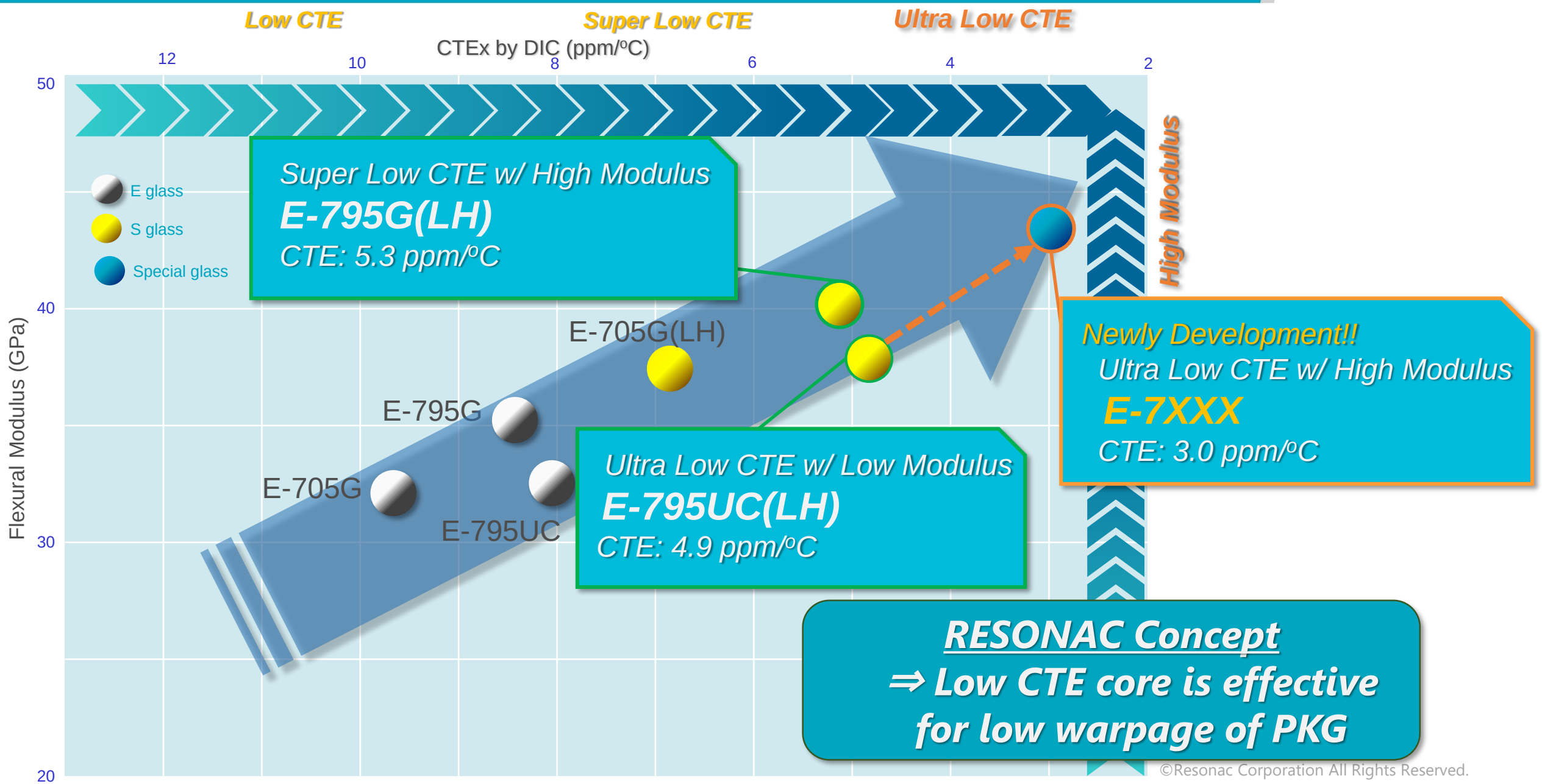
Motivation	Approach	Challenges
High Speed	HSIO on Substrate	Signal Loss ➔ Electrical Property, Body size
Large Capacity of Data Processing	Multi-Core on Die, Large Die ➔ Yield, Manufacturing Cost	Complex Assembly ➔ Chiplet ➔ Power Delivery ➔ Large Body Size
Low Power Consumption	Narrow Pitch ➔ Bump Pitch Scaling	High Density Circuit

Motivation and Challenges in Semiconductors



Challenge in Semiconductors	Requirement To Substrate	Breakthrough During Substrate Process	Proposal / Solution From Material Stand-point
Large body size	Low Warpage High Yield	Warpage Control Shrinkage Control	Low CTE, High Modules Shrinkage Accuracy
High density circuit	Narrow pitch	Fine L/S Fabrication Narrow pitch TH	High Drill-processability
Electrical property	Signal Integration	Pattern, PKG Design	Low Dk/Df
Power delivery	More efficiency Power Delivery	Embedded Multi-layer core (MLC structure)	Super FLAT Core High Resin flow Prepreg

Material Development Direction



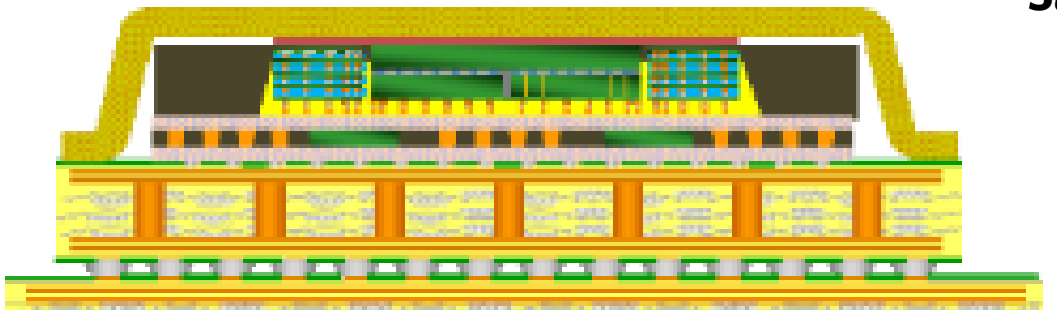
Needs of Organic Core for Large Substrate

Supply Chain Robustness

- Backend process to Base Materials
- Production Capacity
  - Substrate
  - Base Materials (Core, Build-up, etc.)
  - Process (Drilling, Plating, etc.)
  - Process Handling

Knowledge of Packaging

- Warpage Results and Simulation
- Thermal Reliability
- Electrical Reliability
- Stress Simulation



Possibility of Newly Developed Materials

- Knowledge of Resin System
- Lower CTE
- Excellent Electrical Property
- Flatness
- Good Performance of Board Level Reliability
- Friendly for Manufacturing Process

RESONAC

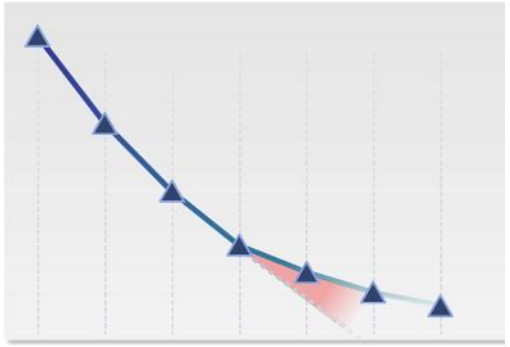
Chemistry for Change

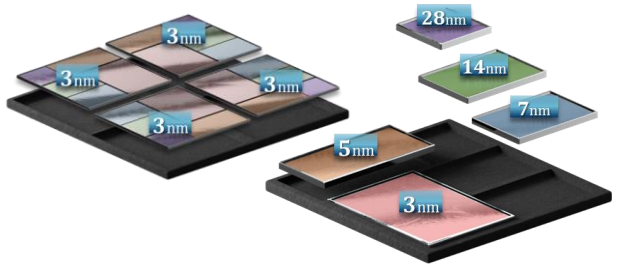
OSTA's Perspective on Chiplets

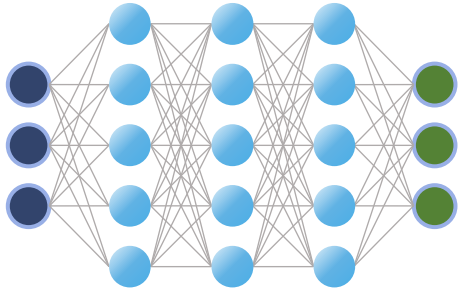
Yu-Po Wang, Ph.D.
Vice President
CRD Center of SPIL
May, 2024

ECTC

Overall Development Shifting for Packaging







Moore's Law
(Difficulty)

- ✓ Scaling of Transistor Density
- ✓ Growing Die Size
- ✓ Higher Cost

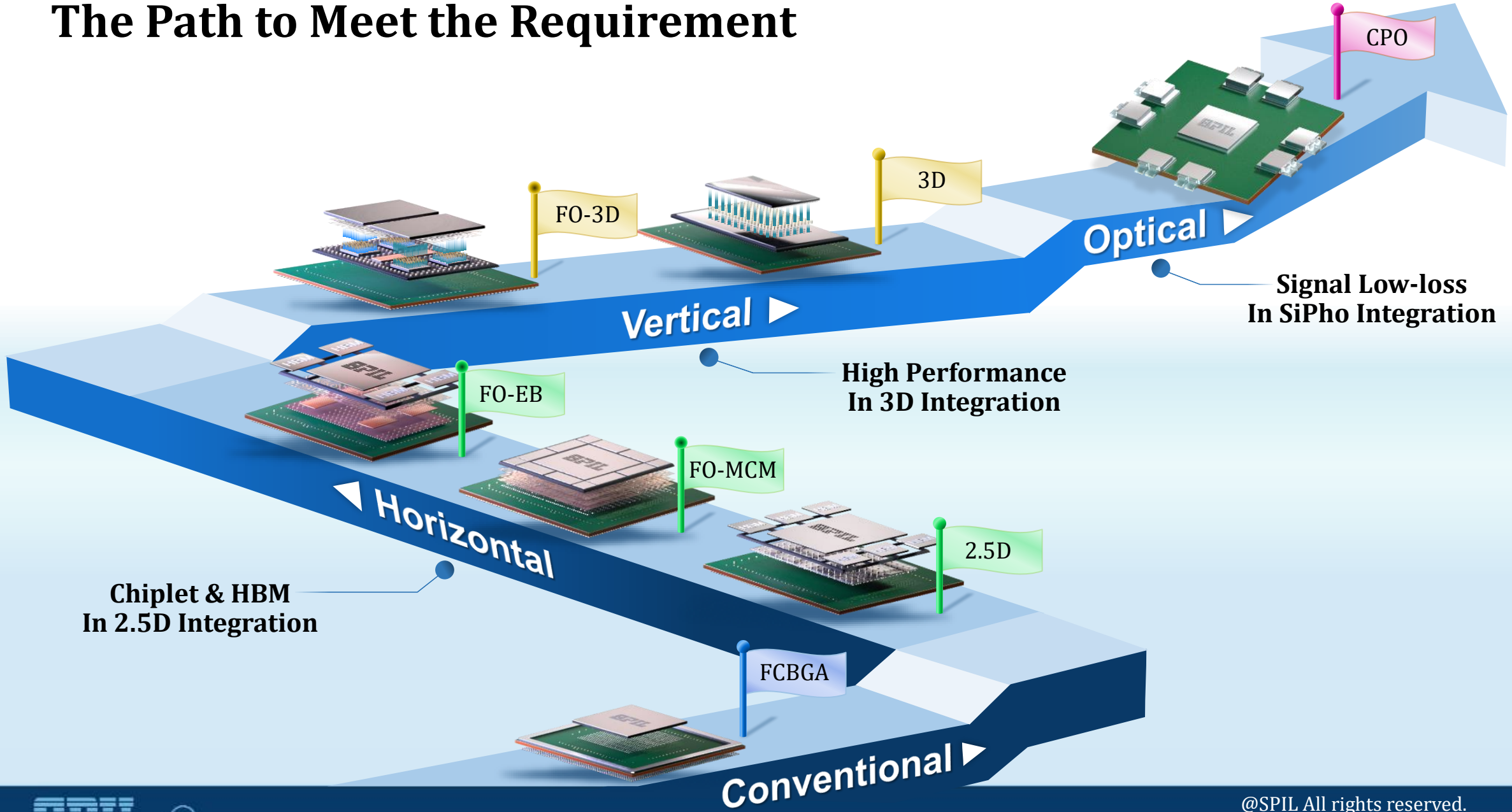
Disaggregation
(Mitigation)

- ✓ Split Die for High Yield
- ✓ Die Partition for Functionality
- ✓ Time to Market

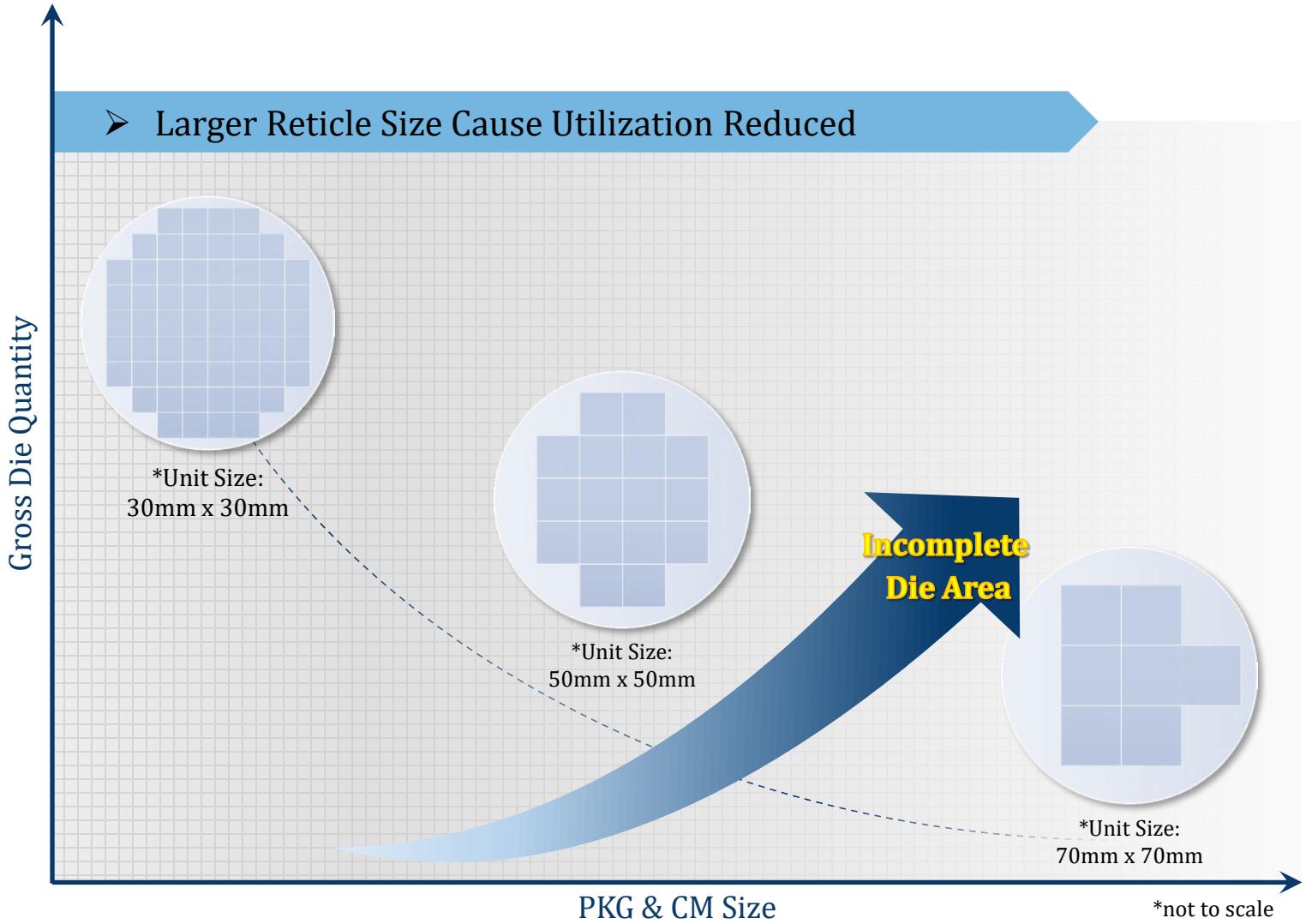
Deep Learning
(High Demand)

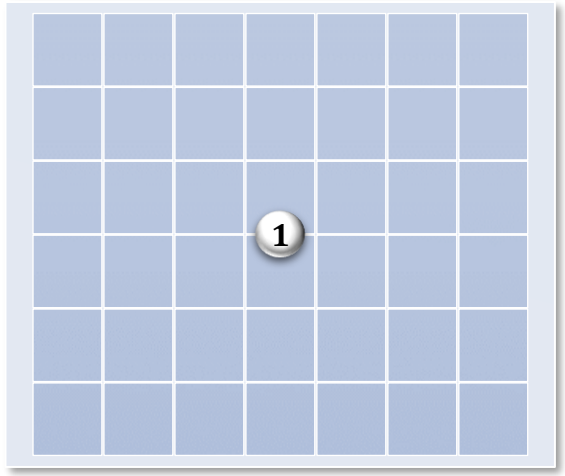
- ✓ Expanding of Memory Capacity
- ✓ High BW for Data Manipulation
- ✓ Performance & Latency

The Path to Meet the Requirement



Utilization Rate Solution

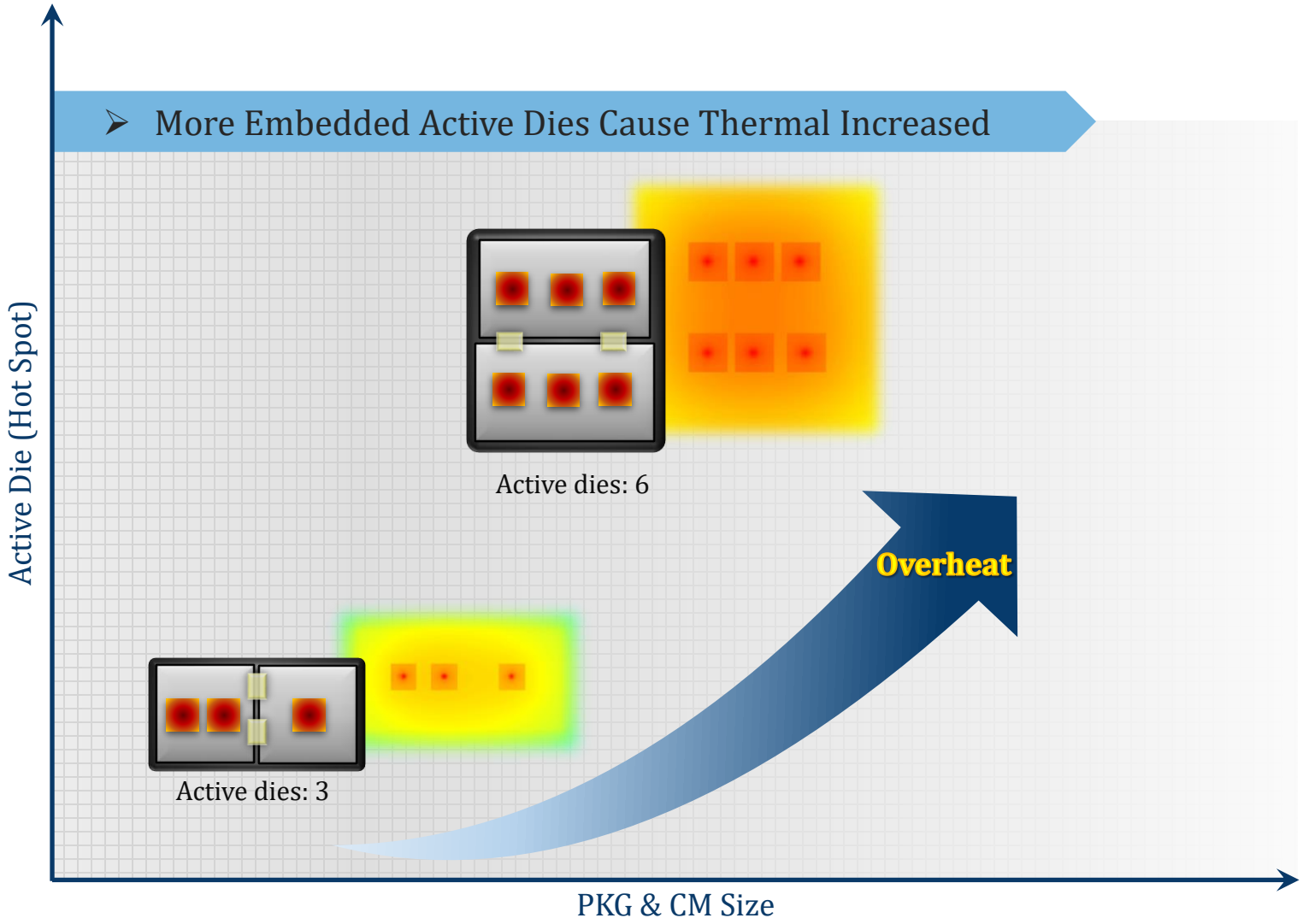


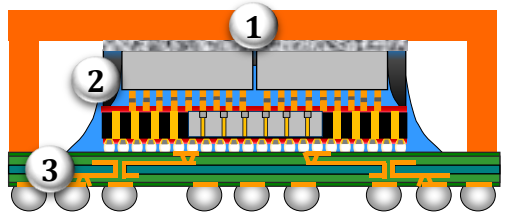


✓ Utilization Improved Directions:

1. Adopting Panel Form Design

Thermal Solution

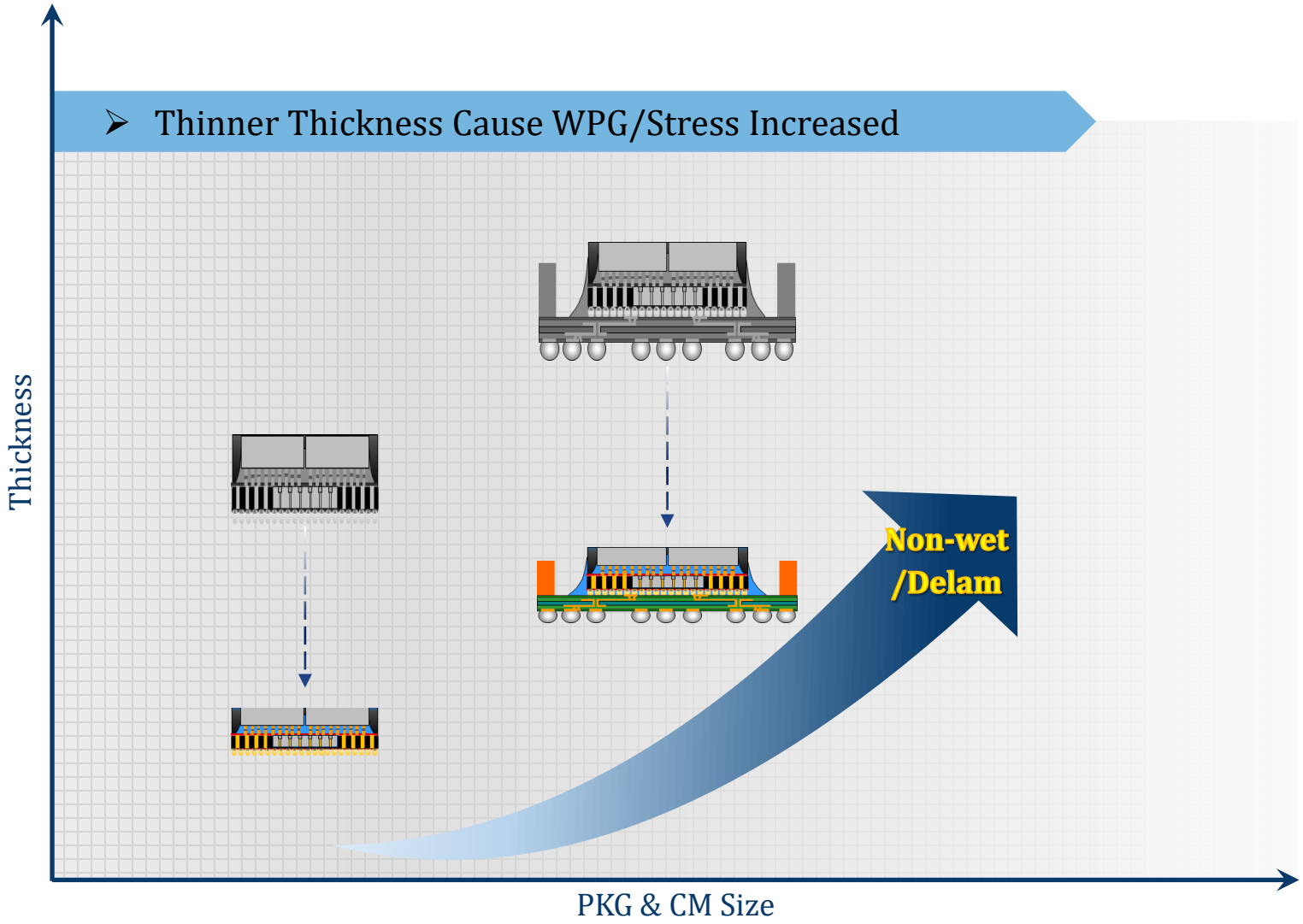


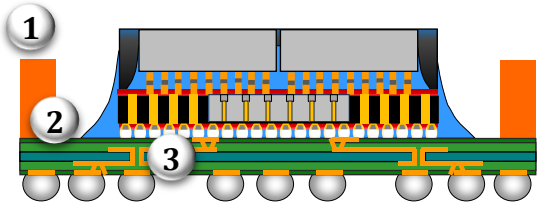


✓ Thermal Dissipation Improved Directions:

1. **High Thermal Conductivity TIM (BSM w/ In-TIM)**
2. **High Thermal Conductivity EMC**
3. **Core Thickness/Cu Coverage of Substrate**

Warpage Solution

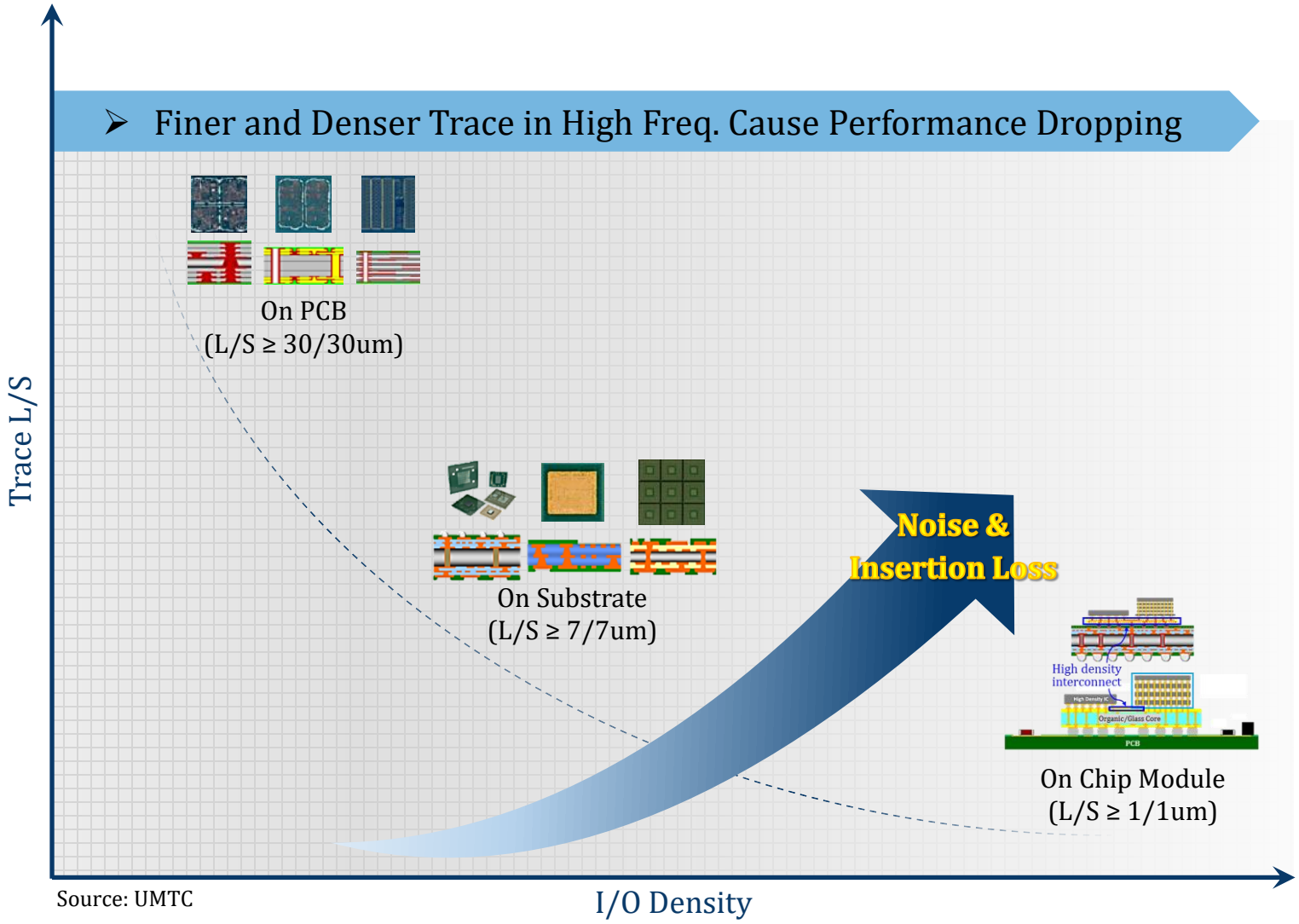




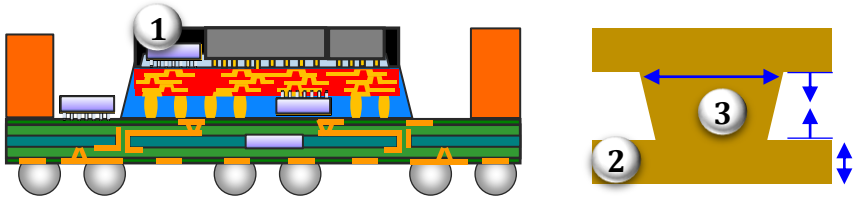
✓ Warpage/Stress Reduced Directions:

1. **Thickness & Footprint of Heat Sink**
2. **Adhesive Modulus**
3. **CTE of Substrate Core/EMC/UF**

Electrical Solution



Source: UMTC



✓ Electrical Optimization Directions:

1. **Integrate Capacitor near Die**

   (Die Side/C4 Side/Embedded in SBT)

2. **Increase RDL Trace Thickness**

3. **Increase Via/Via land Size & Shorten Via Height**

Thank You

www.spil.com.tw

Liquid Metal Ink (LMI_x^{TM}) - A Breakthrough Interconnect Technology

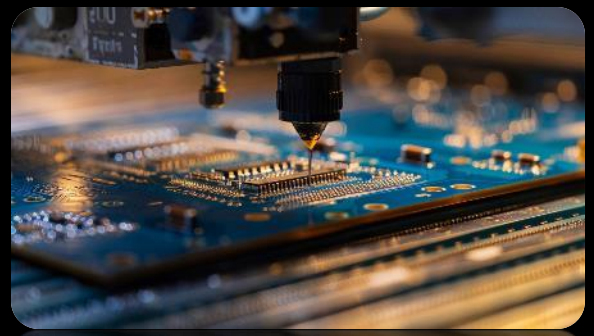
LQDX

Rozalia Beica – Chief Commercial Officer

2024 ECTC | May 28, 2024

Presentation Agenda

Industry Trends



- Semiconductor Industry
- Information Age / AI & HPC

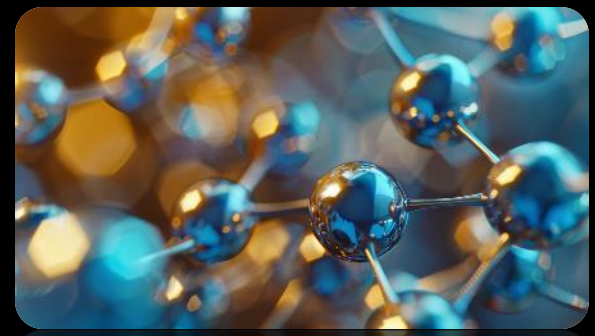
Current Challenges

- Increased Complexity
- High Density Interconnects

LQDX Introduction

- Introduction
- Technology

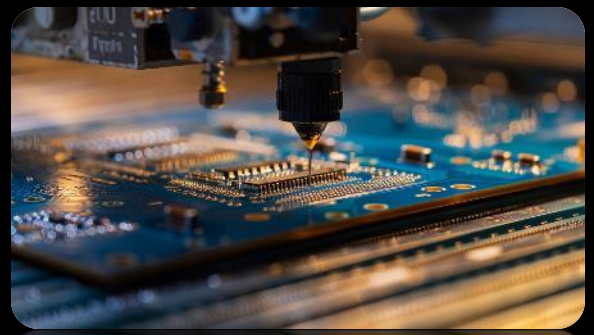
Our Solutions



- High Density Interconnects
- The Road to 1um

Presentation Agenda

Industry Trends



- Semiconductor Industry
- Information Age

Current Challenges

- Increased Complexity
- High Density Interconnects

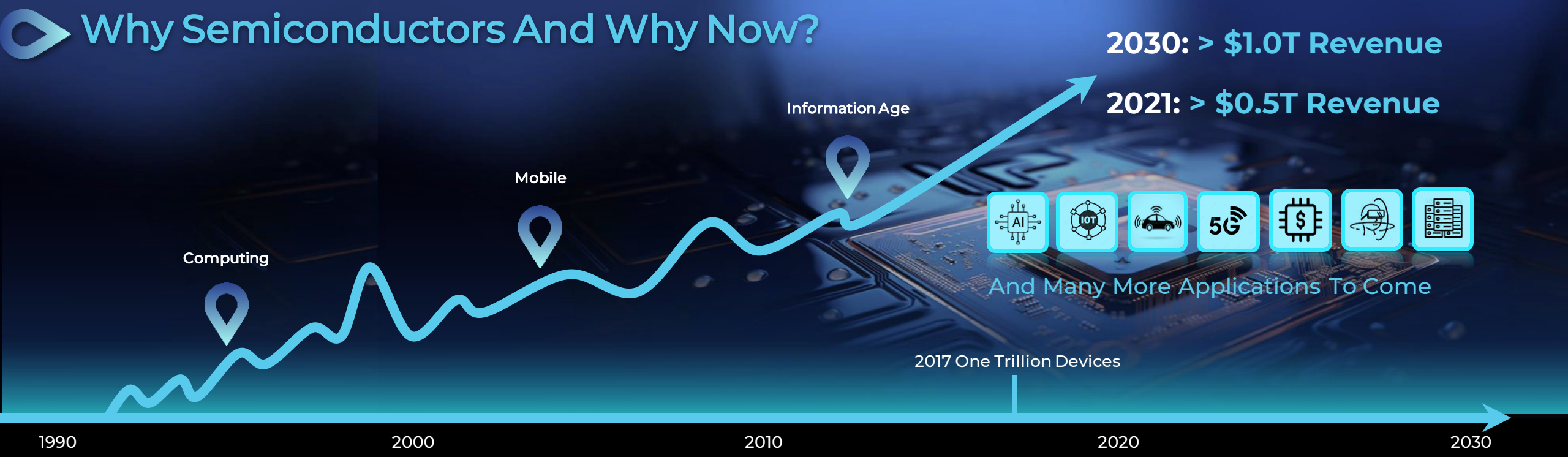
LQDX Introduction

- Introduction
- Technology & IP

Our Solutions

- High Density Interconnects
- The Road to 1um

Why Semiconductors And Why Now?



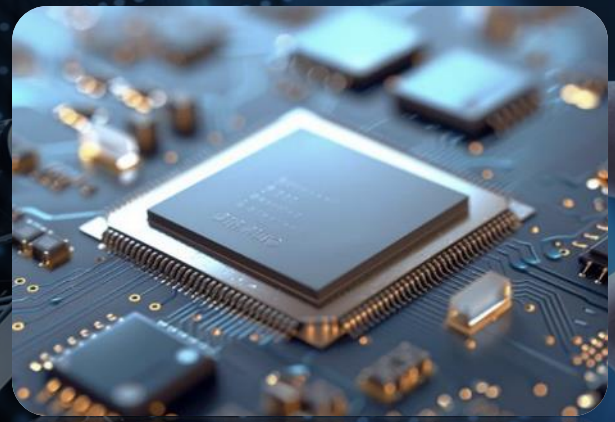
The semiconductor industry has never seen anything like this at any time in its history!

- In the past, there was always One Key Technology driving the roadmap: e.g. PC -> Mobile -> Smartphone -> Information Age
- Now there are multiple growth technologies ramping at the same time: AI, 5G, Datacenter, VR/AR, IIoT, Autonomous Driving, etc.
- AI & HPC are driving an unprecedented market inflection, and many processes and materials are needed to satisfy the demand
- All of this also being catalyzed by government investments worldwide

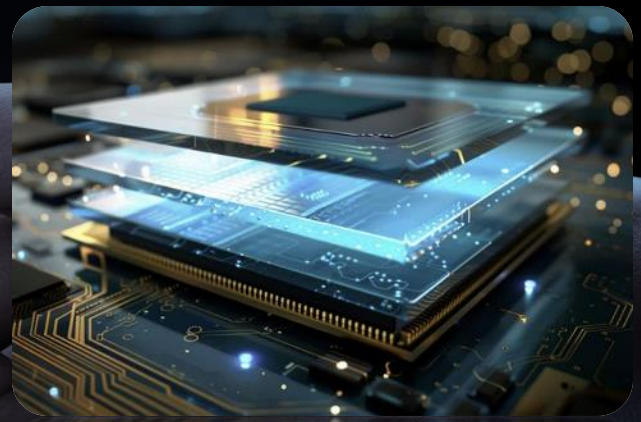
AI Will Drive, Like Never Before, Computing & Memory Needs, Customization

AI / HPC is Driving a Transformative Era in Chiplet Technology & Packaging

- **Chiplets:** a modular approach to system design that is performance driven and cost-effective, customizable and scalable to different computing applications
- The true potential of chiplets is unlocked through advanced packaging solutions and heterogeneous integration
- The economics of chiplet adoption are linked with the cost and maturity of the interconnect & packaging solutions



Single Chip FCBGA



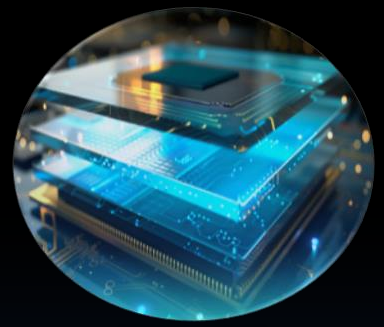
Multi-Chip / Chiplet Packaging

Chiplets Reshaping the Landscape of Advanced Packaging, Driving the Growth of Heterogeneous Integration

High Performance Processors Need High Performance IC Substrates

AI / HPC Driving the Trend Towards Significantly Bigger and More Complex Substrates

- Increased substrate size
- Increased layer count
- More advanced interconnects
- Embedding technologies
- Multi-core substrates
- Glass substrates



Ultra-High-Density Organic Substrates

Fine L/S – demand of a very thin and uniform copper is becoming more and more important

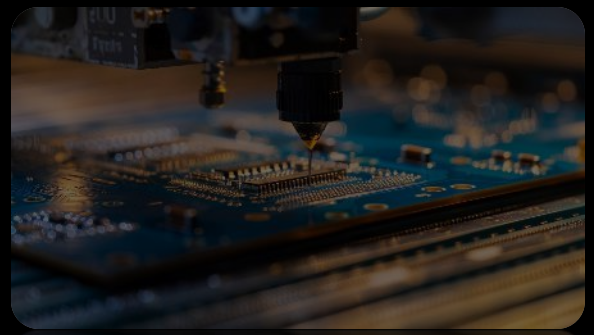
Main Challenges:

- Low roughness / no desmear / adhesion promoters
- Thin Cu seed deposition
- Advanced patterning & via formation processes
- Minium etching /no undercut after seed removal

Computing Growing Exponentially, Faster than Interconnect Improvement & Developments

Presentation Agenda

Industry Trends



- Semiconductor Industry
- Information Age

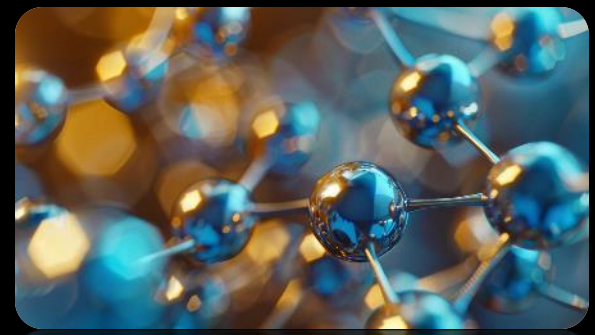
Current Challenges

- Increased Complexity
- High Density Interconnects

LQDX Introduction

- Introduction
- Technology

Our Solutions



- High Density Interconnects
- The Road to 1um

A Silicon Valley Nanomaterials Company Focused On Interconnect Technologies for Advanced Packaging & Substrates

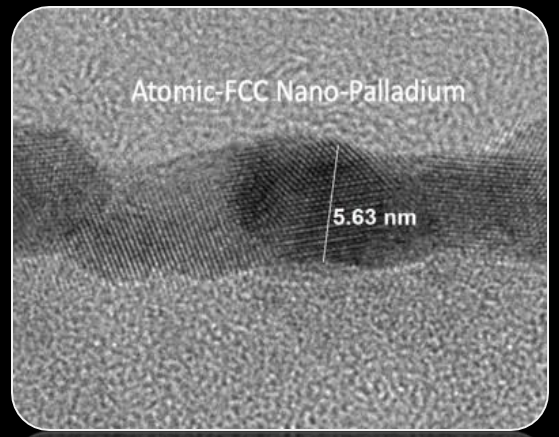
Incubated At Stanford Research Institute.

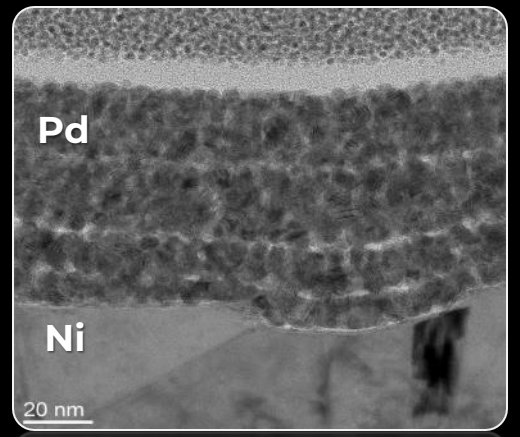
Engineered At Averatek / LQDX Santa Clara.

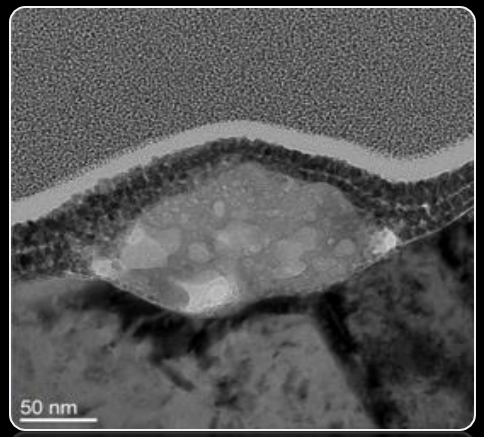
Patented Nano-Inks for AI & HPC Driven Advanced Semiconductor Interconnect

Nano Conformal Deposition Of Atomic Palladium

- Atomic Pd: very thin, nano-layers of conformal Pd deposition (≤ 5nm)
- Atoms will follow the contour very well
- Conformal – difficult to do with PVD

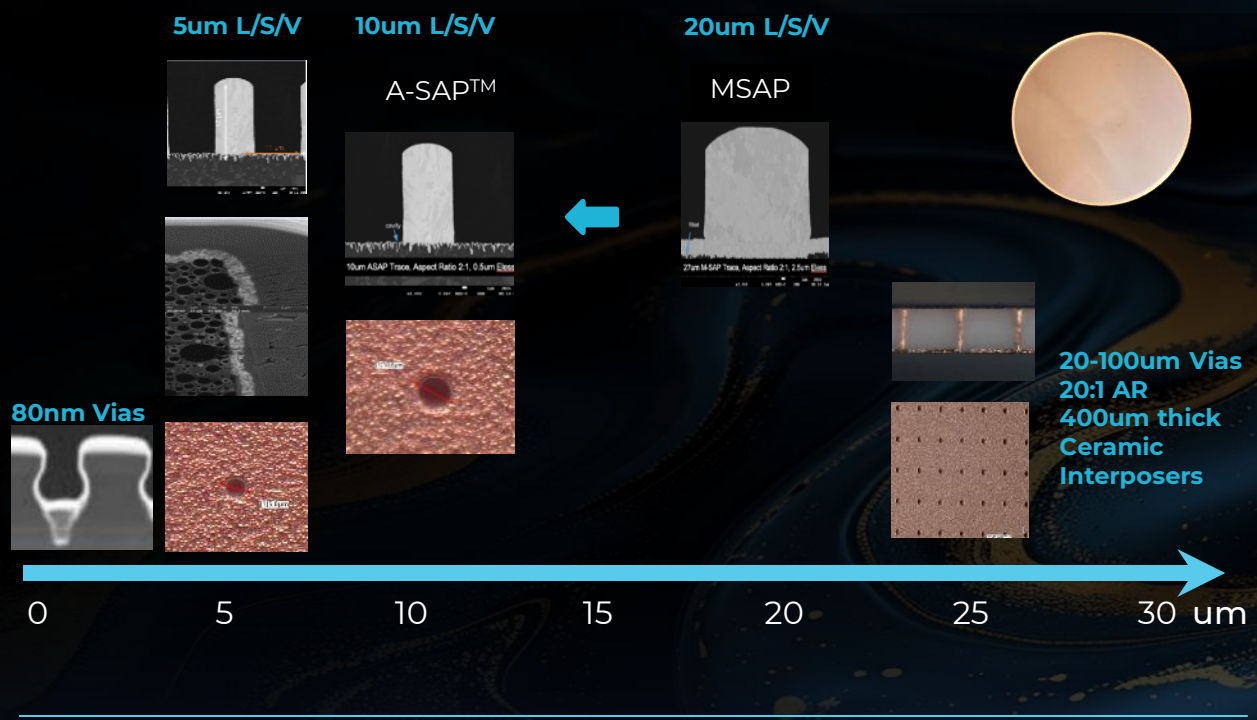






LMI Has a Molecular and Compositional Architecture that Enables Atomic Pd Deposition on the Nano Contours of Substrates

Enabling Advanced Circuits on the Largest Range of Substrates



- **Ultra Thin**: a few nanometers thick **(≤ 5nm Pd vs 100nm PVD)**
- **Ultra Dense**: fully packed nano film enabling uniform initiation of e-less copper **(80nm Cu vs 200-300nm PVD)**
- **Ultra Conformal**: complex surfaces at nanometer scale, **high AR (20:1)** features (TSVs)
- **Ultra Compatible**: adheres to advanced substrates and wide range of materials (Build-up Film, PID, LCP, BT, PTFE, Ceramics, FR4, Flex)
- **Ultra Flexible**: works with pure metals & alloys

Lowest Cost of Adoption And Easy Adoption & Integration into Existing Wet Processing Lines

Driven By Our Passion For Innovation & Engineering, We Are Pushing The Boundaries In Interconnect Technologies

Substrate Interconnect Scale Roadmap

Source: IEEE, Georgia Tech, SEMI, 2022

Materials	Application	Min. Features (um)	2018	2020	2022	2025	2028	2031	2034
Organic Laminate	FCBGA	Bump Pitch	130/100 40/80 30/60	110/100 30/60 20/40	110/100 30/60 20/40	100/90 20/40 15/30	100/90 20/40 15/30	90/80 20/40 15/30	90/80 20/40 15/30
		L/S	9/12	9/12	8/8	5/5	5/5	5/5	5/5
		uVia Diam	50	50	40	30	30	20	20
	CHIPLET (fan-out, organic interposer)	Bump Pitch	50	50	45	40	40	30	30
		L/S	2/2	2/2	2/2	1.5/1.5	1/1	0.5/0.5	0.5/0.5
		uVia Diam	30	30	20	10	10	5	5
Silicon	CHIPLET (2.5D, 3D)	Bump Pitch	40	40	35	30	30	20	20
		L/S	0.6/0.6	0.6/0.6	0.6/0.6	0.5/0.5	0.4/0.4	0.3/0.3	0.2/0.2
		uVia diam	0.6	0.6	0.6	0.5	0.4	0.3	0.2

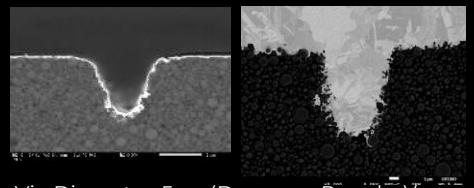
OUR STRATEGIC FOCUS: Enabling The Roadmap to ≤1um L/S using Wet Processing

The Roadmap To 1um

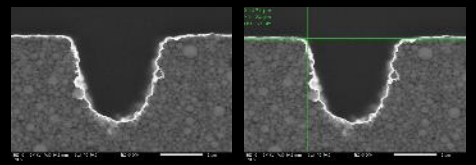
Building Integrated Process for Advanced Interconnects using Wet Process Seed Deposition

Test Vehicle Preparation → ABF Lamination → Via Formation → Desmear / Cleaning → Pd Catalyzation → E-less Cu → PR Patterning → Cu ECD → PR Removal → Seed Removal

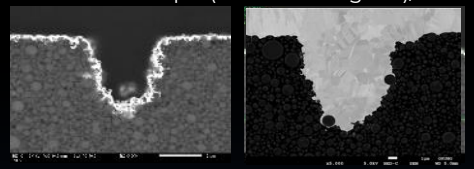
Via Diameter 5µm (Desmear Light)



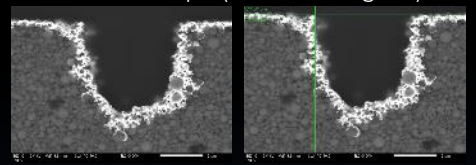
Via Diameter 8µm(Desmear Light)



Via Diameter 5µm(Desmear Regular)



Via Diameter 8µm(Desmear Regular)



ABF Build up Film — AJINOMOTO

Pd Catalyzation — LQDX

E-less Cu — OKUNO (OKUNO CHEMICAL INDUSTRIES CO. LTD.)

Integration of Process Steps & Materials & Characterization

- 1-5um L/S
- 5-20um microvias
- Via formation: using various technologies
- Patterning: stepper vs laser direct imaging
- Photoresist: dry and liquid films
- Electrical characterization & reliability testing

AJINOMOTO

LQDX

UYEMURA

ABF laminated wafers & seeded with 2nm Pd & 100nm E-less Cu
45nm roughness

Summary

- **Unique Atomic Seed Metallization** chemistry suite, enabling very uniform deposition of palladium, gold, copper and other semiconductor metals.
- **Palladium seed metal is the bedrock of every printed circuit made**, including the most advanced substrates, and **the roadmap demands feature sizes of <5um**.
- **LMI$_x$® already proven at 5um,** our focus is now scaling it into the IC substrates, organic interposer, fan-out and TSVs
- Our seed-metallization technologies are a critical tool in the new Heterogeneous Integration toolbox that can bring **a disruptive leap in interconnects**

US PCB Capabilities
75/75um => 25/25um

Advanced IC Substrates HVM (Asia)
8/8um

LQDX LMI
5/5um => 1um L/S

LMI$_x$™: Meeting Today The Needs Of Next Generation IC Substrates

Liquid Metal Ink (LMI_x^{TM}) - A Breakthrough Interconnect Technology

For additional information:
Rozalia Beica
Rozalia@lqdx.com
info@lqdx.com
M: 669.335.6912

Solving New Design Challenges from Chiplet to Multi-Die System

Kenneth E. Larsen, Synopsys

IMPORTANT NOTICE

IMPORTANT NOTICE

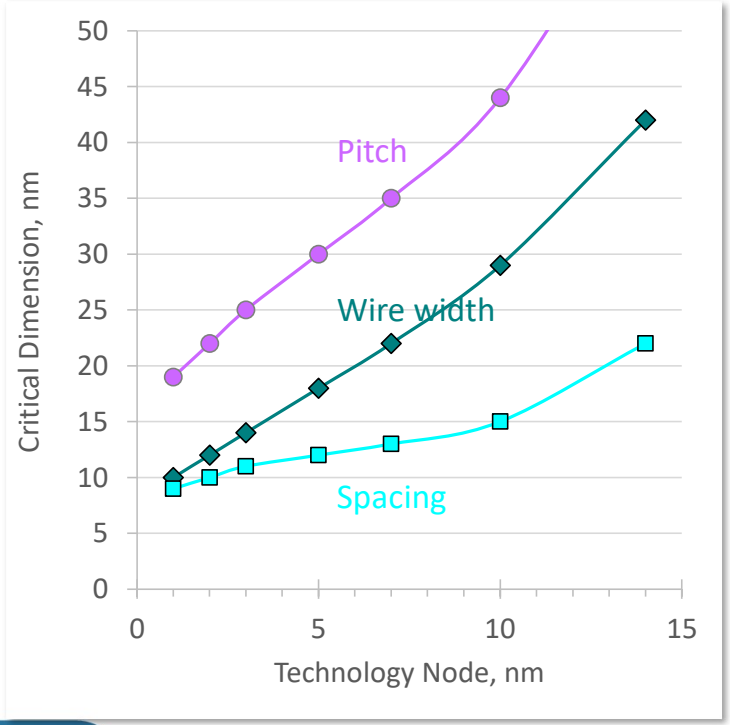
In the event information in this presentation reflects Synopsys' future plans, such plans are as of the date of this presentation and are subject to change. Synopsys is not obligated to update this presentation or develop the products with the features and functionality discussed in this presentation. Additionally, Synopsys' services and products may only be offered and purchased pursuant to an authorized quote and purchase order or a mutually agreed upon written contract with Synopsys.

The Drive to Miniaturization

- The trend foreseen by Richard Feynman “There is plenty of room at the bottom” 1959
- As miniaturization approaches its [physical] limit, performance will come from software, algorithms, and **Multi-Die design**
- Multi-Die design makes dozens of pieces of silicon behave as **one superchip**

From Chiplet to Multi-Die

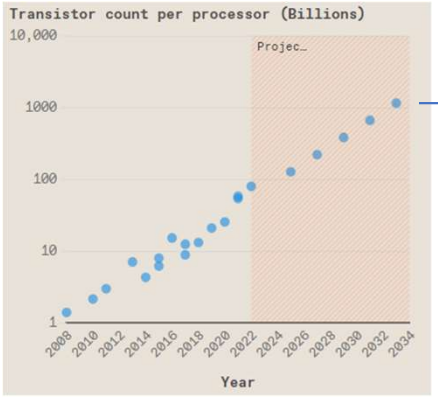
On-chip interconnect scaling
Historical and expected minimum metal wires



Ref: SSDM 2022 Short Course on PPAC of 2DIC & 3DIC. V Moroz, Synopsys

Transistor density scaling
2.85x with CFET vs. current 3nm Fin FET

Scaling silicon CMOS beyond 1nm Complementary FET (CFET) is an attractive device architecture over Fin FET design and will enable density of five hundred million transistor per mm² for logic, and one billion bits SRAM per mm², limited by routing

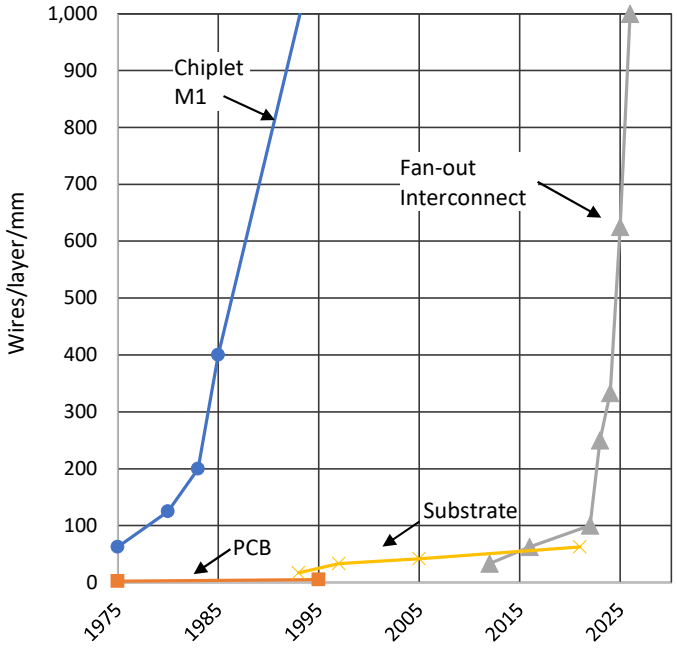


Ref: Towards 1 trillion transistors IEEE Spectrum, TSMC

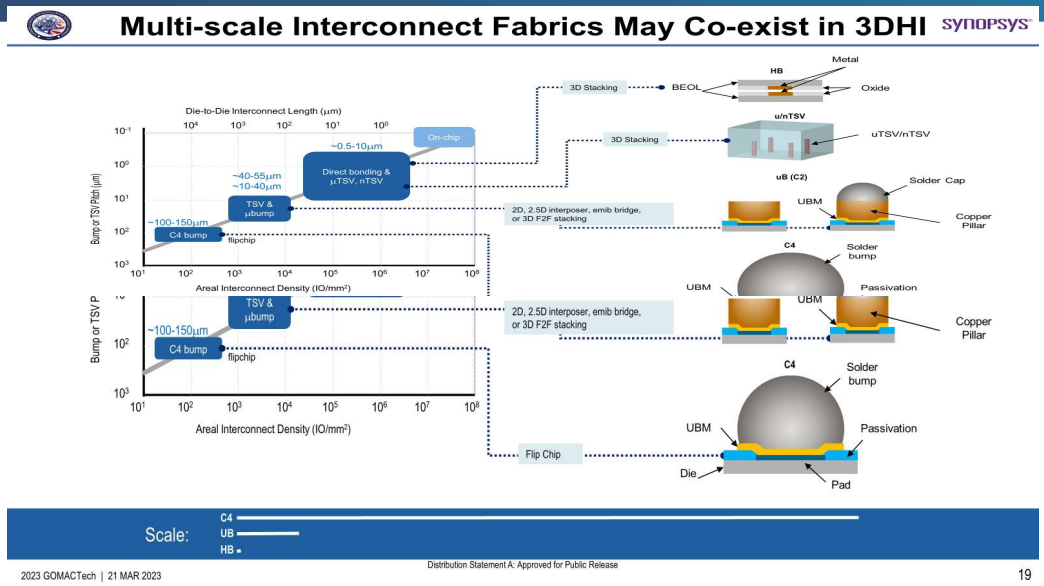
1.2 Trillion transistors per processor

Multi-Die Design

Multi-Die Design



SNUG23: Deca Enable next-gen fan-out interconnect design with IC-style EDA



GOMACTech 23 The New Era of Innovation in 3DHI Microsystems K. Larsen, Synopsys

Multi-Die requirements:

- *Need more vertical connections: direct die bonds, vias, ubumps,…*
- *Need vertical connections to connect any blocks – die, interposer, dielectric,..*
- *Need more wires: Silicon Interposer, Bridge, fan-outs…*
- *May/not have interposer, bridges, ubumps…*
- *Interposers can be any materials…*
- *Vias going through silicon/interposer/dielectric ~TSV,TIV,TDV..*
- *Dies can be stacked*
- *Dies can be in any material*

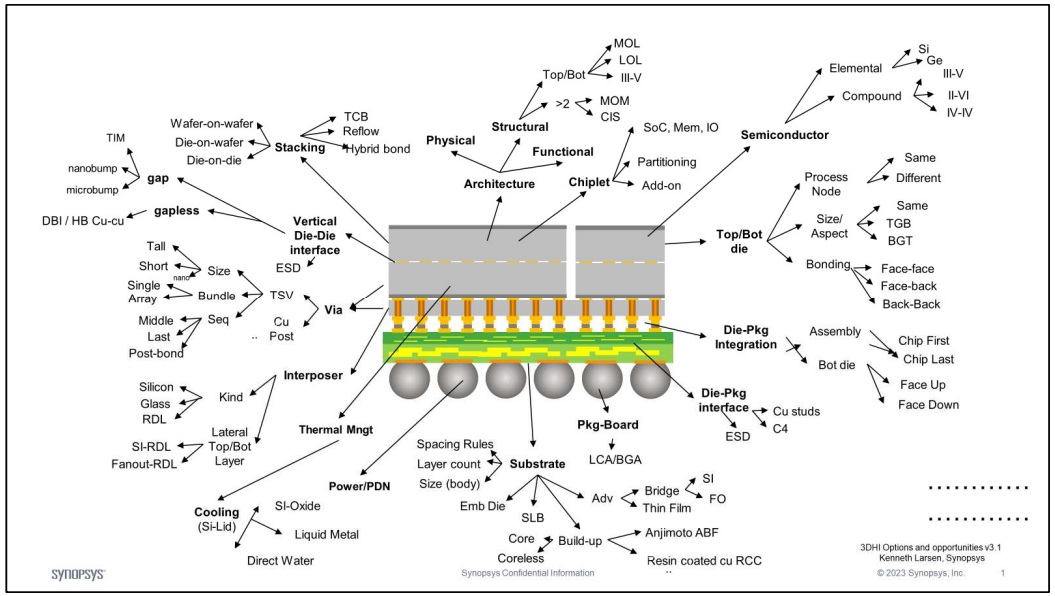
Multi-Die Design Trends And Challenges

Multi-Die Design Trends (ex)

Element	2023 (SOTA)	2030
Power / current density, efficiency	600W TDP , ~1A/mm2, 60-70%	2000W TDP, 2-5A/mm2, >90%
Die IO density	10K/mm2 (10um pitch)	20M/mm^2
Die BW	30Tbps/mm2	500Tbps/ mm^2
Die HBM, Count, ub/count, ub/pitch (x,y,z, 11x11mm2, 720um)	12hi, 8x, 7775, 96x110um	16hi, 16x <60x on SoW, >60x PLP
Capacitors	MiM >500nf/mm2, DTC >5uf/mm2	On-die MiM: >1 uf/mm2, DTC >10uf/mm2
VR	Pkg: 5V IVR (LDMOS/GaN) MB:48V	Pkg:48-12V (GaN)
Silicon interposer / RDL interposer / Package substrate body size	2900 mm2, -, 4844 mm^2	2900 mm2, 5000 mm^2, >120x120mm
Silicon interposer bump pitch, line W/S, via diameter	30um, 0.5/0.5um, 0.6um	20um, 0.3/0.3um, 0.2um
RDL interposer/FO bump pitch, line W/S, via diameter, # Layer(top/bot)	50um, 1/1um, 40um, 10um, 4/2	30um, 0.5/0.5um, 5um, 7/3
Recon fanout L/S	1.8um, wafer level, start panel level	<1um, WLP, PLP
Pkg substrate bump pitch w/wo single route btw bumps Full GA, Staggered	100um, 90um ; 20/40 um,15/30um	90um,80uml 20/40um,15/30um
Pkg substrate, line W/S, via diameter, chip-package copper pillar, Layers	5/5um, 30um, 25um, 8-20	5/5um, 20um, 25um, >25
Die in substrate pitch	Die: 90um, HBM<50um	Die: 70um. HBM<30um
D2W Assembly	Reflow, move to TCB	25um - 20um TCB
D2D Assembly (HCB)	5um	<1um (incl. Organic FO Pkg)
RDL/Substrate components/IPD, pitch	Si-bridge, caps, inductors, 100um	IVR, 65um
Substrate core thickness	400-1000 um	>1500um

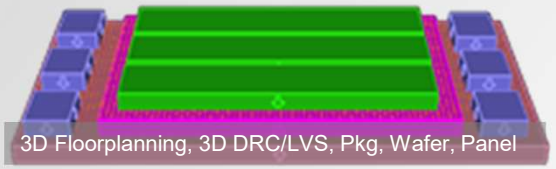
Ref IRDS, public industry reports, Synopsys .

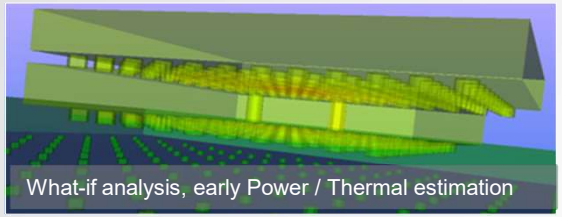
Multi-Die Design Knobs (ex)

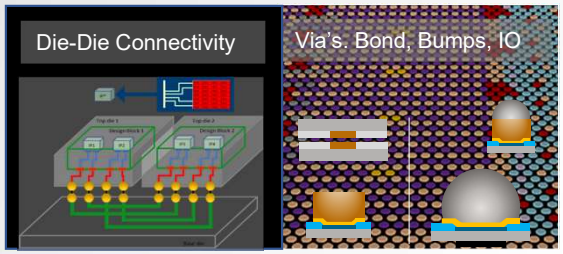


Superchip Design Enablement

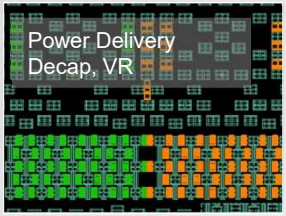
Multi-Die Planning

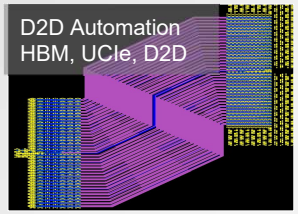


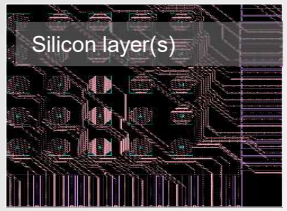


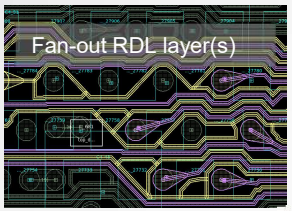


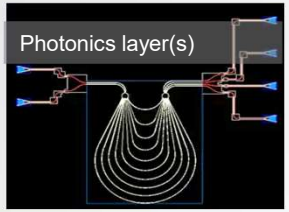
Automation

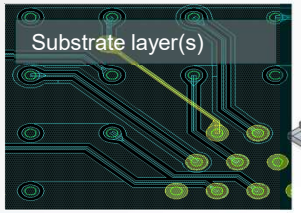




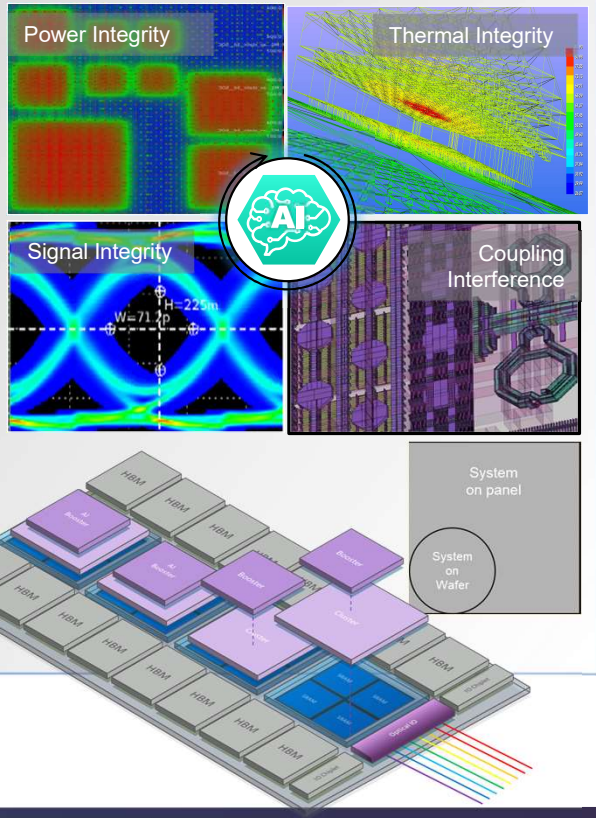








Optimization



Ref: Synopsys 3DIC Compiler Platform

Thank You